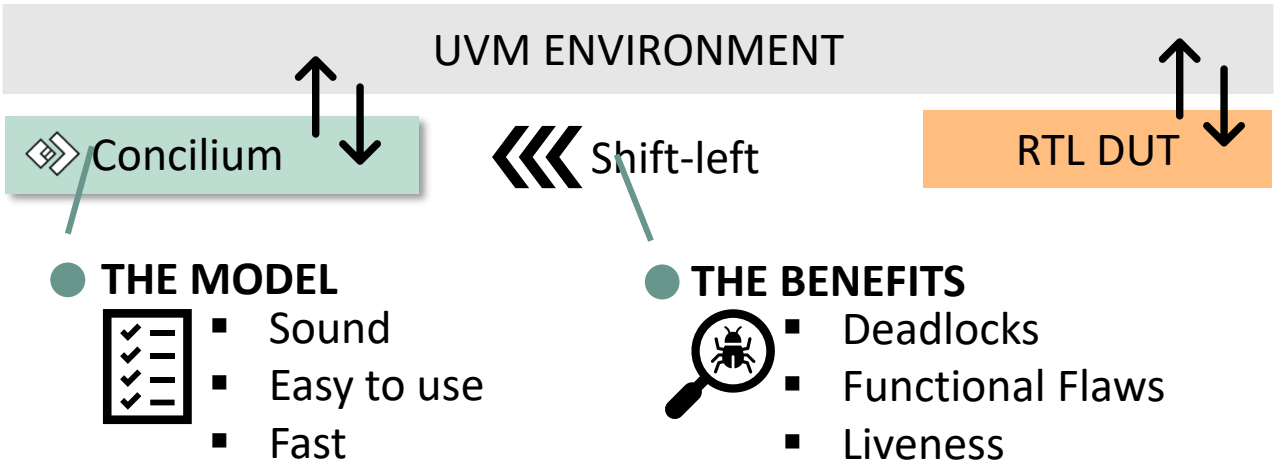
LUBIS EDA

SMART IP GENERATION

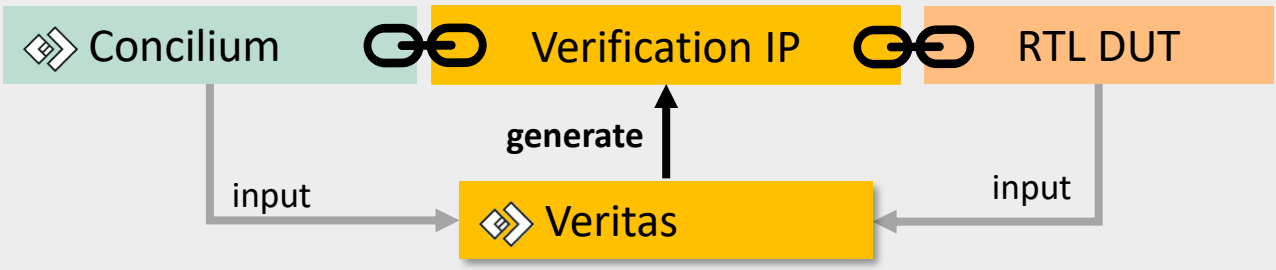
FAST COVERAGE CLOSURE

Use our sound, simple and fast Concilium models to obtain your coverage goals. Simulate at the system level and detect hard to find bugs before you hand off your design. No more bug escapes!



CERTAINTY FOLLOWS AUTOMATION

Our innovative Verification IP generation allows you to establish a link between the Concilium models and the Design Under Test. This uncovers implementation bugs, helps your team to pinpoint the root cause of a functional flaw and results in a complete line and state coverage.



A POWERFUL VERIFICATION IP

Simulation

SVA module that checks valid behavior of the DUT with your existing regression tests.

Property Checking

Use the VIP to exhaustively check your design. 100% functional coverage, no escapes.

Let's start
a new project together

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